SVR ENGINEERING COLLEGE

Approved by AICTE & Permanently Affiliated to JNTUA

Ayyalurmetta, Nandyal – 518503. Website: www.svrec.ac.in

Department of Electronics and Communication Engineering

DIGITAL COMMUNICATION SYSTEMS LABORATORY

III B.Tech (ECE) I Semester

2019-20

STUDENT NAME	
ROLL NUMBER	
SECTION	

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Department of Electronics and Communication Engineering

DEPARTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

ACADEMIC YEAR: 2019-20

This is to certify that the bonafide record work done by

*Mr./Ms.*_____ *bearing*

*H.T.No.*_____ *of III B.Tech I Semester in the* **Digital**

Communication Systems Laboratory

Faculty In-Charge **Head of the Department**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

B.Tech – III-I Sem (E.C.E)

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(15A04508) DIGITAL COMMUNICATION SYSTEMS LABORATORY

Minimum of Ten experiments to be conducted (Five from each Part-A&B)

HARDWARE EXPERIMENTS (PART – A)

1. Time division multiplexing.
2. Pulse code modulation.
3. Differential pulse code modulation.
4. Delta modulation.
5. Frequency shift keying.
6. Differential phase shift keying.
7. QPSK modulation and demodulation.

SOFTWARE EXPERIMENTS (PART-B)

Modeling of Digital Communications using MATLAB

1. Sampling Theorem – verification.
2. Pulse code modulation.
3. Differential pulse code modulation.
4. Frequency shift keying.
5. Phase shift keying.
6. Differential phase shift keying.
7. QPSK modulation and demodulation.

Equipment required for Laboratories:

1. RPS	-	0 – 30 V
2. CROs	-	0 – 20 M Hz.
3. Function Generators	-	0 – 1 M Hz
4. RF Generators (3 Nos.)	-	0 – 1000 M Hz.

5. Multimeters
6. Lab Experimental kit for Pulse Code Modulation (Experiment No.3 of part –A)
7. Required Electronic Components (Active and Passive) which include required ICs
8. Arbitrary Wave form generators/ PNS generators – 2 Nos. (to generate digital data at required data rates)
9. Licensed **MATLAB R 2016a** software for 30 users with required tool boxes.

ECE DEPT VISION & MISSION PEOs and PSOs

Vision

To produce highly skilled, creative and competitive Electronics and Communication Engineers to meet the emerging needs of the society.

Mission

- Impart core knowledge and necessary skills in Electronics and Communication Engineering through innovative teaching and learning.
- Inculcate critical thinking, ethics, lifelong learning and creativity needed for industry and society
- Cultivate the students with all-round competencies, for career, higher education and self-employability

I. PROGRAMME EDUCATIONAL OBJECTIVES (PEOS)

PEO1: Graduates apply their knowledge of mathematics and science to identify, analyze and solve problems in the field of Electronics and develop sophisticated communication systems.

PEO2: Graduates embody a commitment to professional ethics, diversity and social awareness in their professional career.

PEO3: Graduates exhibit a desire for life-long learning through technical training and professional activities.

II. PROGRAM SPECIFIC OUTCOMES (PSOS)

PSO1: Apply the fundamental concepts of electronics and communication engineering to design a variety of components and systems for applications including signal processing, image processing, communication, networking, embedded systems, VLSI and control system

PSO2: Select and apply cutting-edge engineering hardware and software tools to solve complex Electronics and Communication Engineering problems.

III. PROGRAMME OUTCOMES (PO'S)

1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and

management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

IV. COURSE OBJECTIVES

- To familiarize the students with basic analog communication systems.
- Integrate theory with experiments so that the students appreciate the knowledge gained from the theory course.
- Understand all types of analog modulation / demodulation principles.
- Substantiate pulse modulation techniques.
- To design and implement different modulation and demodulation techniques.
- To write and execute programs in MATLAB to implement various modulation techniques.

V. COURSE OUTCOMES

After the completion of the course students will be able to

Course Outcomes	Course Outcome statements	BTL
CO1	Design and conduct experiments, analyze and interpret data of PCM & DPCM	L1
CO2	Design and conduct experiments, analyze and interpret data of DM & TDM	L4
CO3	Design and conduct experiments, analyze and interpret data of FSK, PSK, DPSK & QPSK	L3
CO4	Design different communication applications using digital modulation techniques	L2

VI.COURSE MAPPING WITH PO'S AND PEO'S

Course Title	PEO1	PEO2	PEO3	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
DC Lab	**3**	**3**	**2**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**1**	**2**	**2**	**2**	**2**

VII MAPPING OF COURSE OUTCOMES WITH PEO'S AND PO'S

Course Outcomes	PEO1	PEO2	PEO3	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO-1	**3**	**3**	**2**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**1**	**2**	**2**	**2**	**2**
CO-2	**3**	**3**	**2**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**1**	**2**	**2**	**2**	**2**
CO-3	**3**	**3**	**2**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**1**	**2**	**2**	**2**	**2**
CO-4	**3**	**3**	**2**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**1**	**2**	**2**	**2**	**2**

LABORATORY INSTRUCTIONS

1. While entering the Laboratory, the students should follow the dress code. (Wear shoes and White apron, Female Students should tie their hair back).

2. The students should bring their observation book, record, calculator, necessary stationery items and graph sheets if any for the lab classes without which the students will not be allowed for doing the experiment.

3. All the Equipments and components should be handled with utmost care. Any breakage or damage will be charged.

4. If any damage or breakage is noticed, it should be reported to the concerned in charge immediately.

5. The theoretical calculations and the updated register values should be noted down in the observation book and should be corrected by the lab in-charge on the same day of the laboratory session.

6. Each experiment should be written in the record note book only after getting signature from the lab in-charge in the observation notebook.

7. Record book must be submitted in the successive lab session after completion of experiment.

8. 100% attendance should be maintained for the laboratory classes.

Precautions.

1. Check the connections before giving the supply
2. Observations should be done carefully

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DIGITAL COMMUNICATION SYSTEMS

LAB MANUAL

Exp.No. 1	**TIME DIVISION MULTIPLEXING**
Dt.	

AIM: To Study and verify the process of time division multiplexing & demultiplexing with two different frequency signals.

APPARATUS:
1.TDM trainer kit
2. CRO
3. Patch cards
4. BNC probes

THEORY:

The Sampling Theorem provides the basis for transmitting the information contained in a band limited message signal m (t) as a sequence of samples of m (t) taken uniformly at a rate that is usually slighter higher than the nyquist rate. An important feature of the sampling process is a conservation of time. That is, the transmission the message samples engages the communication channel s for only a fraction of the sampling interval on a periodic basis, and in this way some of the time interval between adjacent samples is cleared for use by other independent message sources on a time shared basis.

Multiplexing:

It is the process of combining signals from different information sources so that they can be transmitted over a common channel. Multiplexing is advantageous in cases where it is impracticable and uneconomical to provide separate links for the different information sources. The price that has to be paid to acquire this advantage is in the form of increased system complexity and bandwidth. Most commonly used methods of multiplexing are 1. Frequency division multiplexing (FDM) 2. Time division multiplexing (TDM)

Time Division Multiplexing:

Time division multiplexing is the process of combining the samples from different information signals, in time domain so that they can be transmitted over the same channel. The fact utilized in TDM technique is that there are large intervals between the message samples. The samples from the other sources can be placed within these time intervals. Thus every sample is separated from other in time domain. The time division multiplexing system can be simulated by two rotating switches, one at transmitter and the other at receiver. The two wipers rotate and establish electrical contact with one channel at a time.

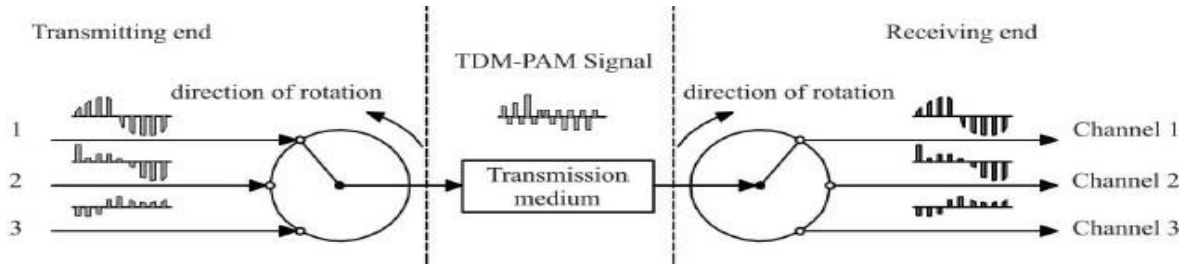


Figure 1: Block Diagram of TDM Transmitter

Each signal is sampled over one sampling interval and transmitted one after the other along a common channel. Thus part of message 1 is transmitted first followed by part of message 2, message 3 and then again message 1 so on. It can be anticipated from above process that the
To establish synchronization, the receiver needs to know:
a. Frequency/ rate of operation at transmitter.
b. Sample identification.
This increases the transmitter and receiver complexity and cost.

The TDM system is highly sensitive to dispersion in the common channel, that is, to variations of amplitude with frequency or lack of proportionality of phase with frequency. Accordingly, accurate equalization of both magnitude and phase response of a channel is necessary to ensure a satisfactory operation of the system. Unlike FDM, TDM is immune to non linearities in the channel as a source of cross talk. The reason for this is, the different message signals are not simultaneously applied to the channel. The primary advantage of TDM is that several channels of information can be transmitted simultaneously over a single cable.

BLOCK DIAGRAM/CIRCUIT DESCRIPTION:

Block diagram:

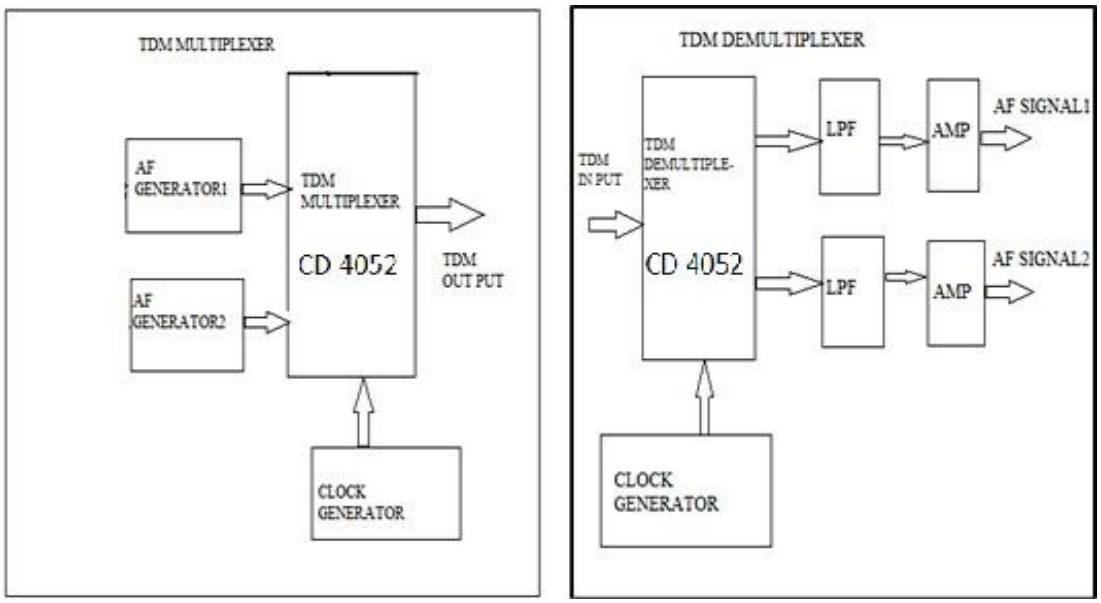
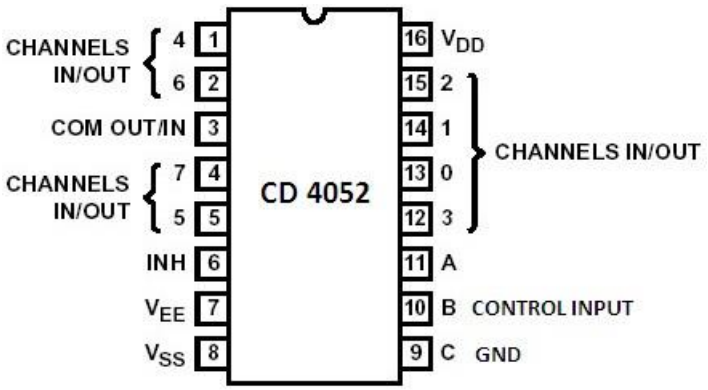


Fig 2: BLOCK DIAGRAM OF TDM MULTIPLEXER AND DEMULTIPLEXER

PIN Diagram of CD4052:



Regulated power supply: This consists of a bridge rectifier followed by Capacitor filters and three terminal regulators 7805 and 7905 to provide regulated DC voltages of ± 5V @ 300 mA to the on board circuits. These supplies have been internally connected to the circuits, so no external connections are required for operation.

Audio Frequency (AF) Signal generators: Sine wave signals of 400 Hz & 200 Hz are generated from AF generator-1 and AF generator -2 respectively to use as a message signals to be transferred. These generators are Op-Amp based Wein-bridge Oscillators using IC TL084. IC TL084 is a FET input general purpose Operational Amplifier. Amplitude control is provided in the circuit to vary the output amplitude of AF signal.

Clock generator: A TTL compatible clock signal of variable frequency is provided on board to use as a control (timing) signal to the multiplexer & de-multiplexer circuits. This circuit has been designed based on the application of CMOS integrated circuits in linear mode. Here IC 4069 is used as an active device. 4069 is a CMOS hex inverters integrated circuit. Three inverters are used to form a oscillator and other three are connected as a buffer to isolate oscillator from output and to improve current capability.

Logic source: As name indicates this provides logic signals i.e. Logic'1' (represents +5V) and Logic '0' (represents 0V). This is a simple two way switch followed by a buffer circuit and this is applicable in single step operation of multiplexer & de-multiplexer circuits.

Low pass filters: These are a series of simple RC networks provided on board to reconstruct the message signals from PAM signals i.e. output of the de-multiplexer. RC values are chosen such that the cutoff frequency would be at 200 Hz.

Amplifiers: These are Op-amp (IC TL084) based non-inverting variable gain amplifiers provided on board to amplify the recovered message singles i.e. output of the Low pass filter to desired level. Amplitude control is provided in circuit to vary the gain of the amplifier between 0 and 10. AC/DC Switch facilitates to couple the input signal through capacitor or directly to the amplifier input.

2- Channel TDM multiplexer: CD 4052 IC is a 4 channel analog multiplexer/de-multiplexer and is used as an active component in this circuit. One of the control signals (pin 9) of 4052 is grounded so that 4052 will act as a two channel multiplexer and other control input (pin 10) is being terminated as control signal of TDM Multiplexer. The message signals that has to be multiplexed are to be connected to CH_1 (pin 12) and CH_2 (pin 14) inputs of the CD 4052. Multiplexed output is taken from pin 13. TL084 has been used as a buffer at input of the CD4052 in order to avoid loading effect on signal sources. For pin configuration and other operating conditions of IC 4052 you can go through the data sheet provided along with manual.

2-Channel TDM De-multiplexer: IC CD 4052 is a 4 channel analog multiplexer/de-multiplexer and is used as an active component in this circuit. One of the control signals (pin 9) of 4052 is grounded so that 4052 will act as a two channel de-multiplexer and other control input (pin 10) is being terminated as control signal of TDM de-multiplexer. The TDM signal that has to be de-multiplexed is connected to a common input (pin 13). De-multiplexed outputs are taken as CH1 (from pin 14) and CH2 (pin 12). Outputs of the de-multiplexer can be connected to low pass filters for smoothing the output. TL084 has been used as a buffer at input of the CD4052 in order to avoid loading effect on signal sources. For pin configuration and other operating conditions of IC 4052 you can go through the data sheet provided along with manual.

Synchronization: De-multiplexer at the receiver should be operate in synchronize with the multiplexer which is at transmitter in order to recover the original signals without any loss. In actual communication system a synch signal will be added to the TDM signal and the clock generator at receiver will be triggered with the synch signal.

-

EXPERIMENTAL PROCEDURE:

Multiplexer:

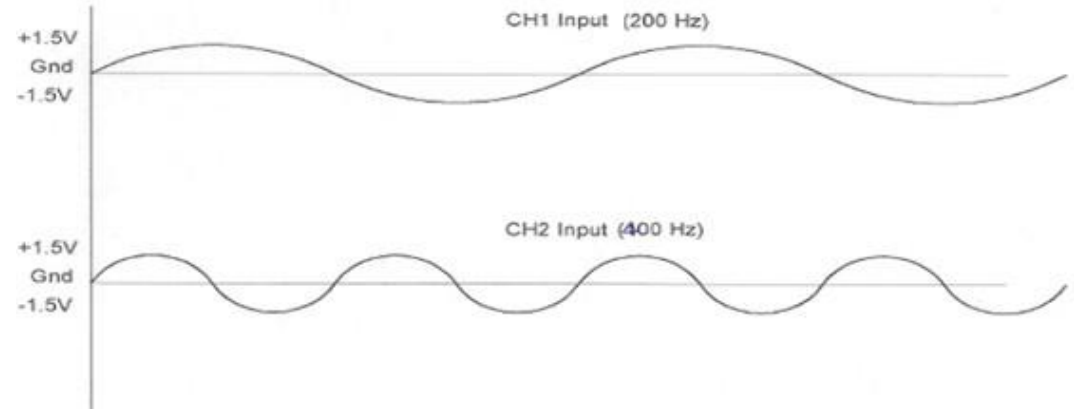
1. Connect the trainer (AET-55M) to the mains and switch on the power supply.
2. Observe the output of the AF generator-1 using CRO, it should be a Sine wave of 400 Hz frequency with 3Vpp amplitude.
3. Observe the output of the AF generator-2 using CRO it should be a Sine wave of 200 Hz frequency with 3Vpp amplitude.
4. Verify the operation of logic source with multimeter/scope, output should be +5V in logic1 position and 0V in logic 0 position.
5. Observe the output of the Clock generator using C.R.O it should be a Square wave of 500 Hz to 15 KHz frequency with 5Vpp amplitude.
6. Now connect the CH1 & CH2 Inputs of the TDM multiplexer to the outputs of the AF Generator1 and 2 respectively.
7. Connect Control input of the TDM multiplexer to the output of the logic source.
8. Put control signal (logic source) at logic 1 condition and observe the output of the TDM multiplexer with the help oscilloscope, by this we can notice that the output of the TDM multiplexer is a signal which has been connected to CH1 input. In this condition the signal at CH2 input has no effect on multiplexer output.
9. Similarly put logic source at logic 0 position and observe the output of the TDM multiplexer. Now notice that the output of the TDM multiplexer is a signal which has been connected to the CH2 input and the signal at CH1 input has no effect on multiplexer output.
10. Now disconnect logic source and connect clock output to the control input.
11. Observe TDM wave form using C.R.O at different values of clock frequency, input signal voltage levels and sketch them.

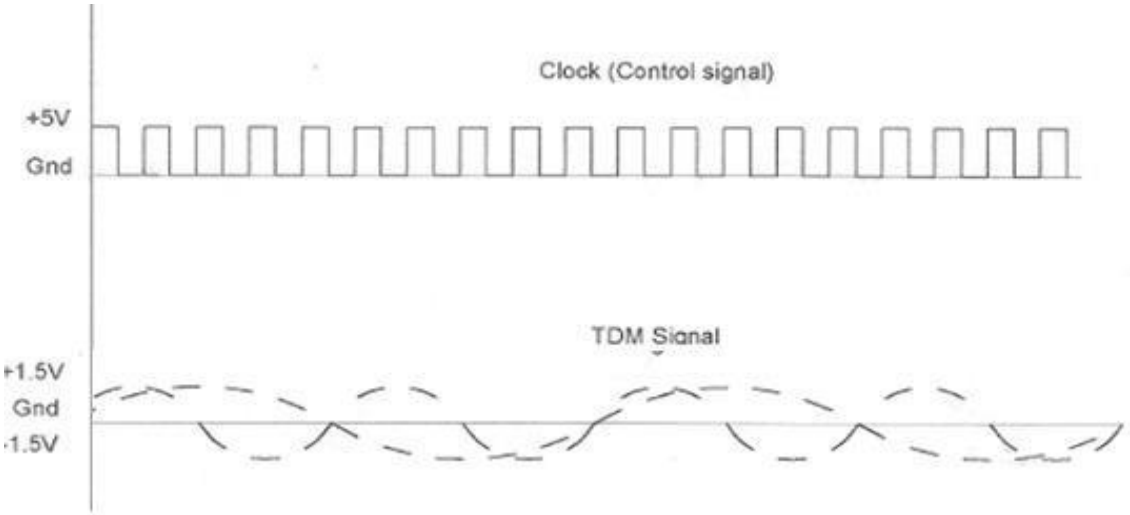
Note1: After setting the clock frequency and input signals to desire values put storage scope in STOP mode so that you can view stable display of waveforms.

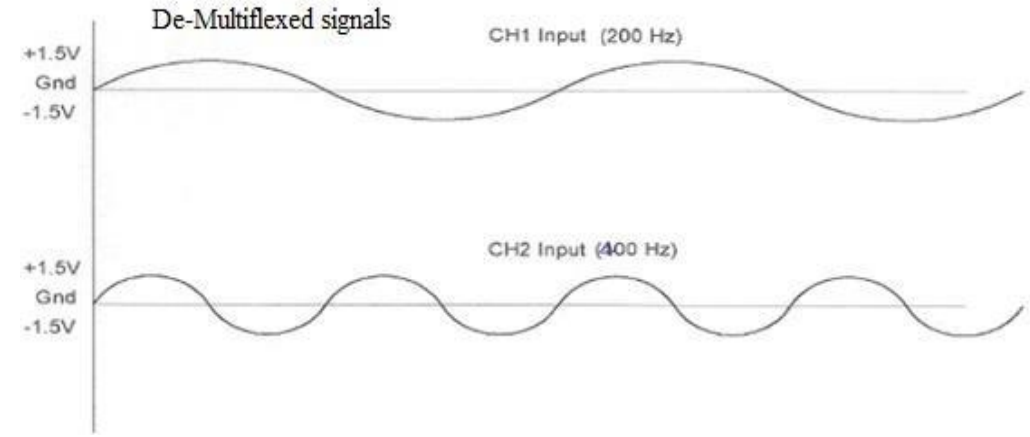
De-multiplexer:

12. Connect TDM (PAM) signal to input of TDM de-multiplexer from TDM multiplexer (i.e. AET-55M) with the help of co-axial cable (supplied with trainer).
13. Put logic source to 1 position and observe CH1 and CH2 outputs. You can notice that the entire TDM signal is transferred to CH1 output and has no signal at CH2 output.
14. Similarly put logic source to 0 position and observe CH1 and CH2 outputs. Now the entire TDM signal is transferred to CH2 output and has no signal at CH1 output. By the above two steps you can notice that the entire TDM signal is transferred to CH1 output when control input is 1 and to CH2 output when control input is 0.
15. Now disconnect logic source and connect clock from the transmitter (i.e., AET- 55M) through a coaxial cable.
16. Observe CH1 and CH2 outputs. You will notice that the outputs are natural top sampled PAM signals.

Waveforms:


CH1 Input (200 Hz)
+1.5V
Gnd
-1.5V
CH2 Input (400 Hz)
+1.5V
Gnd
-1.5V


Clock (Control signal)
+5V
Gnd
TDM Signal
+1.5V
Gnd
-1.5V


De-Multiflexed signals
CH1 Input (200 Hz)
+1.5V
Gnd
-1.5V
CH2 Input (400 Hz)
+1.5V
Gnd
-1.5V

OBSERVATION TABLE:

Multiplexing:

Signal	Amplitude	Time Period	Frequency
AF Signal 1			
AF Signal 2			
Clk			
TDM o/p AF_1			
TDM o/p AF_2			

De- multiplexing:

Signal	Amplitude	Time Period	Frequency
AF Signal 1			
AF Signal 2			

RESULT:-

Viva - Questions:

1. Define synchronous TDM**.**
2. Define asynchronous TDM.
3. What is frame in TDM?
4. List out the application of TDM.

Exp.No. 2	**PULSE CODE MODULATION**
Dt.	

Aim: To study the operation of Pulse Code Modulation & Demodulation by using A.C & D.C inputs

Equipment:

1. PCM Modulator trainer
2. PCM Demodulator trainer
3. Cathode Ray Oscilloscope
4. Digital Multimeter.
5. 2 No's of co-axial cables

Theory:

Pulse modulation: A form of modulation in which a pulse train is used as the carrier. Information is conveyed by modulating some parameter of the pulses with a set of discrete instantaneous samples of the message signal. The minimum sampling frequency is the minimum frequency at which the modulating waveform can be sampled to provide the set of discrete values without a significant loss of information. There are different forms of pulse modulations like pulse amplitude modulation (PAM), pulse width modulation (PWM), pulse position modulation (PPM).

PCM: In pulse code modulation (PCM) only certain discrete values are allowed for the modulating signals. The modulating signal is sampled, as in other forms of pulse modulation. But any sample falling within a specified range of values is assigned a discrete value. Each value is assigned a pattern of pulses and the signal transmitted by means of this code. The electronic circuit that produces the coded pulse train from the modulating waveform is termed a coder or encoder. A suitable decoder must be used at the receiver in order to extract the original information from the transmitted pulse train.

Block Diagram/Circuit Description:

Block Diagram:

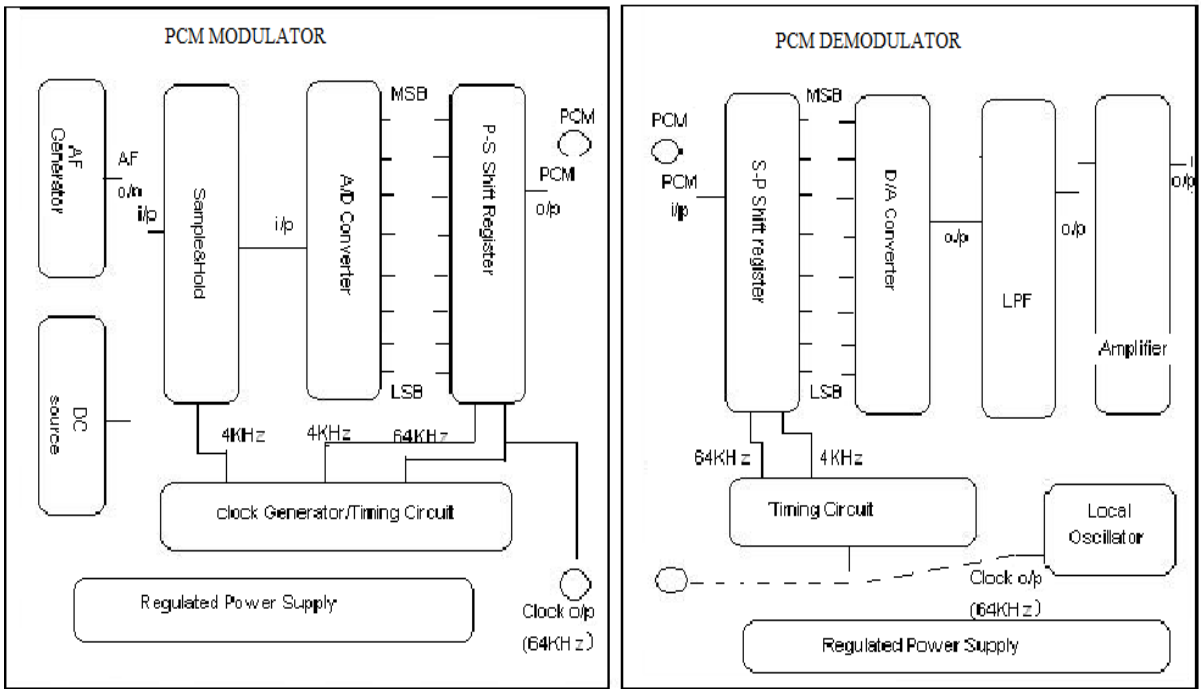


Fig 1: PCM MODULATOR & DEMODULATOR

Regulated power supply: This consists of a bridge rectifier followed by Capacitor filters and three terminal regulators 7805 and 7905 to provide regulated DC voltages of ± 5V and +12V @ 300 mA each to the on board circuits. These supplies have been ***internally connected to the circuits,*** so no external connections are required for operation.

Audio Frequency (AF) Signal generator: Sine wave signal of 200 Hz is generated to use as a modulating (message or information) signal to be transmitted. This is an Op-Amp based Wein bridge Oscillators using IC TL084. IC TL084 is a FET input general purpose Operational Amplifier. Amplitude control is provided in the circuit to vary the output amplitude of AF signal.

Clock generator/ Timing circuit: A TTL compatible clock signal of 64 KHz and 4 KHz frequency are provided on board to use as a clock to the various circuits in the system. This circuit is an astable multivibrator using 555 timer followed by a buffer and frequency dividers.

DC source : A 0 to +5V variable DC voltage is provided on board to use as a modulating signal instead of AF Signal. This is use full to study step by operation of PCM modulation and demodulation. This is a simple circuit consists of potentiometer and fixed power supply.

Low pass filters: This is a series of simple RC networks provided on board to smoothen the output of the D/A converter output (stair case signal). RC values are chosen such that the cutoff frequency would be at 200 Hz.

Amplifiers: This is an Op-amp (IC TL084) based non-inverting variable gain amplifiers provided on board to amplify the recovered message singles i.e. output of the Low pass filter to desired level. Amplitude control is provided in circuit to vary the gain of the amplifier between 0 and 3. AC/DC Switch facilitates to couple the input signal through capacitor or directly to the amplifier input.

Sample & Hold circuit: This block (circuit) is a combination of buffer, level shifting network and sample & hold network. Op-amp IC TL084 is connected as buffer followed by non-inverting summer circuit. One of the inputs of summer is connected a voltage divider network and other being drawn as input. A dedicated sample & hold integrated circuit LF 398 is used as an active component followed by buffer. The LF198/LF298/LF398 is monolithic sample-and-hold circuits which utilize BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate.

Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198 will operate from ±5V to ±18V supplies.

8 Bit A/D Converter: This has been constructed with a popular 8 bit successive approximation A/D Converter IC ADC0808.The ADC0808, data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals. A dedicated 1 MHz clock generator is provided in side this block. For complete specifications and operating conditions please refer the data sheet of ADC0808.

8 Bit Parallel-Serial Shift Register: A dedicated parallel in serial out shift register integrated circuit is used followed by a latch The SN74LS166 is an 8-Bit Shift Register. Designed with all inputs buffered, the drive requirements are lowered to one 74LS standard load. By utilizing input clamping diodes, switching transients are minimized and system design simplified.The LS166 is a parallel-in or serial-in, serial-out shift register and has a complexity of 77 equivalent gates with gated clock inputs and an overriding clear input.

8 Bit Serial-Parallel Shift Register: A dedicated serial in parallel out shift register integrated circuit is used followed by a latch. The SN74LS164 is a high speed 8-Bit Serial-In Parallel-Out Shift Register. Serial data is entered through a 2-Input AND gate synchronous with the LOW to HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all TTL products. For complete specifications and operating conditions please refer the data sheet of SN74LS164.

8 Bit D/A converter: This has been constructed with a popular 8 bit D/A Converter IC DAC 0808. The DAC0808 is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 $I_{REF}/256$. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for I_{REF} >= 2 mA. The power supply current of the DAC0808 is independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range. For complete specifications and operating conditions please refer the data sheet of DAC 0808.

PCM Operation:

The modulating signal is applied to sample & hold circuit. This applied signal will be super imposed by +2.5V DC so that the negative portion the modulating signal will clamped to positive, this process is needed, because input of the A/D Converter should be between 0 and +5V. After level shifting is done the signal will be passed to sample & hold circuit. Sample & hold circuit will sample the input signal during on period of the clock signal and will hold the sampled output till next pulse comes. Sampling rate is 4 KHz in this system.

So input of the A/D converter is a stable voltage of certain level in between 0 and +5V. A/D converter (encoder) will give a predetermined 8 bit code for the sampled input. This entire conversion process will be made at a fast rate as ADC 0808 is operating at high frequency clock i.e. 1MHz.

Coded output of the A/D converter is applied to input of the parallel in serial out register through a latch (74ls373). This shift register is operating at 64 KHz (sampling frequency is 4 KHz, so to shift 8 bits from parallel to serial we need 64 KHz). This output (PCM) is transmitted through a co-axial cable which represents a communication channel.

This 8 bit code is applied to 8 bit D/A converter. Output of the D/A converter will be a staircase signal ling between 0 and +5v. This stair case signal is applied a low pass filter. This low pass will smoothen the staircase signal so that we will get a recovered AF signal.

We can use a voltage amplifier at the output of the low pass filter to amplify the recovered AF signal to desired voltage level.

Procedure:

1. Connect the trainer (AET-68M) to the mains and switch on the power supply.
   Note: From this wave form you can observe that the LSB bit enters the output first.
2. Set the output of the DC source with multimeter/scope; to one of the sampled level and connect it to the A/D converter input and observe the output LED's.
3. Note down PCM output for such a sample based on LED glow or not glow. Take it as binary '1' if LED glows otherwise take it as binary '0'.
4. Compare with theoretical calculations given below.

Theoretical value can be obtained by:

$$\frac{\text{A/D input voltage}}{\text{1 LSB value}} = X_{(10)} = Y_{(2)}$$

Where

1 LSB Value = $V_{ref}/2^n$
Since V_{ref} = 5V and n=8
1 LSB Value = 0.01953

Example:

A/D Input voltage = 4.4 V
= $225.28_{(10)}$
= $1110\ 0001_{(2)}$
So digital output is 1110 0001

Demodulation:

5. Connect PCM signal to the demodulator(S–P shift register) from the PCM modulator (AET- 68M) with the help of coaxial cable (supplied with the trainer).
6. Connect clock signal (64 KHz) from the transmitter (AET–68M) to the receiver (AET-68D) using coaxial cable.
7. Similarly you can try for different values of modulating signal voltage.
8. Observe the output of D/A converter output using multimeter/scope and observer the output LED's.

Sample work sheet:

1. Modulating signal : 4.4 V
2. A/D Output (theoretical) : $1110\ 0001_{(2)}$
3. A/D Output (practical) : $1110\ 0001_{(2)}$
4. S-P Output : $1110\ 0001_{(2)}$
5. D/A Converter output (Demodulated output) : 4.4 V

OBSERVATIONS:

Sampled value 1 : V PCM output: (8 bit binary)

Signal	Amplitude	Time Period	Frequency
D.C input Signal			
Input signal			
Clock 1			
Clock 2			
Demodulated Output			

Waveforms:

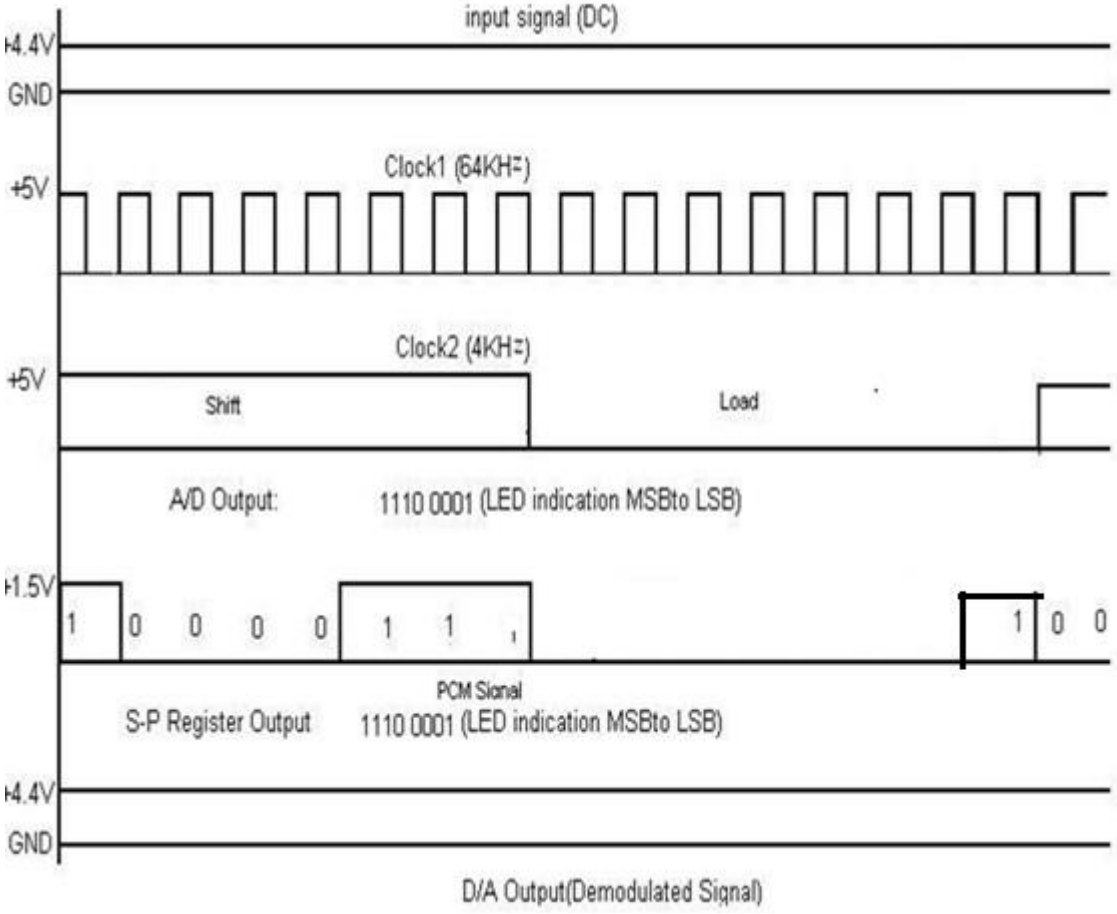


Fig 2: WAVEFORMS OF PCM (DC Input)

PROCEDURE:

1. Switch ON the power supply
2. Open MATLAB software by clicking MATLAB icon on Desktop.
3. Open the editor window and write the program on it.
4. Save the program in workspace as .m file.
5. Run the program and view the graph.

MATLAB CODE:

```
clc
close all
clear all
t = 0:0.0001:20;
c=input('Enter Bit Depth Of PCM Coding:');
part = -1:0.1:1;
codebook = -1:0.1:1.1;
msg = cos(t);
[~,quants] = quantiz(msg,part,codebook;
subplot(3,1,1);
plot(t,msg);
title('Message Signal');
subplot(3,1,2);
plot(t,quants);
title('Quantized Signal');
y = uencode(quants,c);
ybin=dec2bin(y,c);
subplot(3,1,3);
plot(t,y);
title('PCM PLOT');
```

RESULT:-

Viva- Questions:

1. Which noise is occurs in PCM?
2. What is Quantization?
3. What is the advantage of PCM?
4. At which factor bandwidth of PCM depends?

Exp.No. 3	**DELTA MODULATION**
Dt.	

Aim: To Study the operation of Delta modulation and demodulation technique.

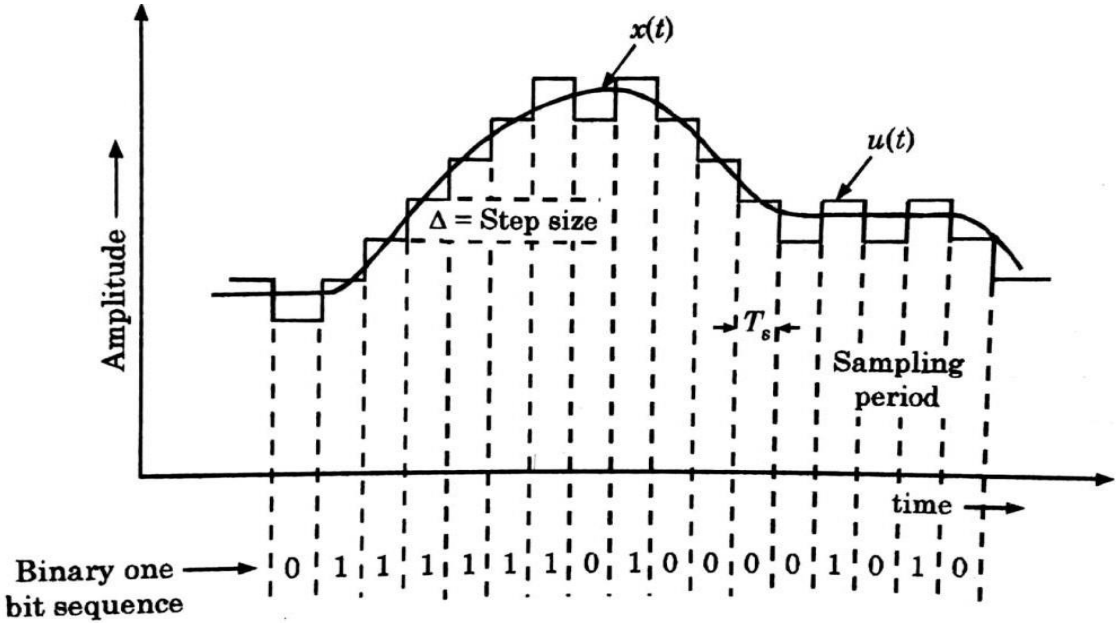
APPARATUS REQUIRED: Demodulation Trainer kit, CRO, patch cards

Theory: Delta modulation is a system of digital modulation developed after pulse code modulation. In this system, at each sampling time, say the K^{th} sampling time, the difference between the sample value at sampling time K and the sample value at the previous sampling time (K-1) is encoded into just a single bit. If signal amplitude has increased, then modulator's output is at logic level 1. If the signal amplitude has decreased, the modulator output is at logic level 0. Thus, the output from the modulator is a series of zeros and ones to indicate rise and fall of the waveform since the previous value.

Delta Modulator: The analog signal which is to be encoded into digital data is applied to the +ve input of the voltage comparator which compares it with the signal applied to its -ve input from the integrator output (more about this signal in forth coming paragraph). The comparator's output is logic '0' or '1' depending on whether the input signal at +ve terminal is lower or greater than the -ve terminals input signal. The comparator's output is then latched into a D-flip-flop which is clocked by the transmitter clock. Thus, the output of D-flip-Flop is a latched 'l' or '0' synchronous with the transmitter clock edge. This binary data stream is transmitted to receiver and is also fed to the uni-polar to bipolar converter. This block converts logic '0' to voltage level of + 4V and logic 'l' to voltage level - 4V. The Bipolar output is applied to the integrator whose output is as follows:

a. Rising linear ramp signal when - 4V is applied to it, (corresponding to binary 1)

b. Falling linear ramp signal when + 4V is applied to it (corresponding to binary 0).The integrator output is then connected to the -ve terminal of voltage comparator, thus completing the modulator circuit. Let us understand the working of modulator circuit with the analog input waveform applied as below:



Delta Modulation Wave form

Block Diagram:-

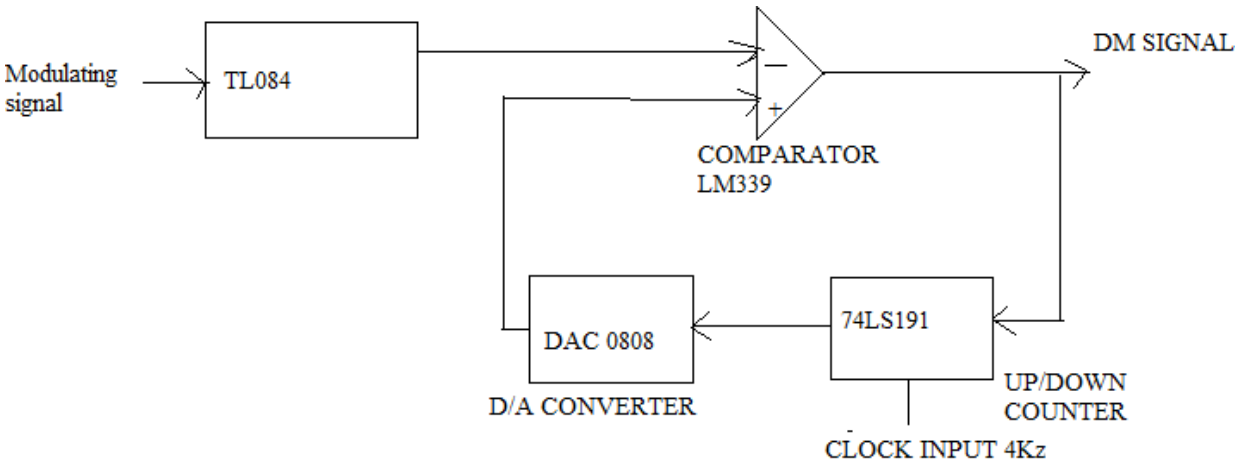
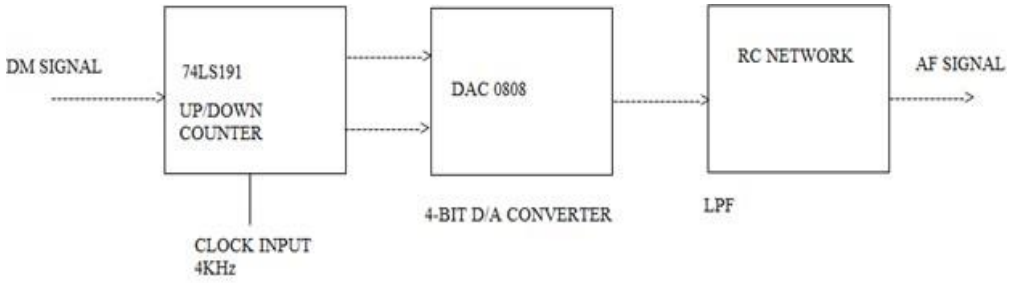


FIG 1: BLOCK DIAGRAM OF DM MODULATOR



BLOCK DIAGRAM OF DM DEMODULATOR

Regulated power supply: This consists of a bridge rectifier followed by Capacitor filters and three terminal regulators 7805 and 7905 to provide regulated DC voltages of ± 5V and +12V @ 300 mA each to the on board circuits. These supplies have been ***internally connected to the circuits,*** so no external connections are required for operation.

Audio Frequency (AF) Signal generator: Sine wave signal of 100 Hz is generated to use as a modulating (message or information) signal to be transmitted. This is an Op-Amp based Wein bridge Oscillators using IC TL084. IC TL084 is a FET input general purpose Operational Amplifier. Amplitude control is provided in the circuit to vary the output amplitude of AF signal.

Clock generator/ Timing circuit: A TTL compatible clock signal of 4 KHz frequency is provided on board to use as a clock to the various circuits in the system. This circuit is an astable multi vibrator using 555 timer followed by a buffer.

Buffer/Signal shaping network: A non inverting buffer using ICTL084 is provided at the input of the DM modulator followed by a level shifting network. Buffer provides the isolation between DM circuit and the signal source. Signal shaping (level shifting network) super imposes the 1.5V DC on incoming modulating signal so that the input of the comparator lies between 0 and +3V maximum.

Voltage comparator: This circuit is build with IC LM339.The LM339 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. Application areas include limit comparators, simple analog to digital converters; pulse, square wave and time delay generators; wide range VCO; MOS clock timers; multi vibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic- where the low power drain of the LM339 is a distinct advantage over standard comparators.

Low pass filters: This is a series of simple RC networks provided on board to smoothen the output of the D/A converter output (stair case signal). RC values are chosen such that the cutoff frequency would be at 100 Hz.

Amplifiers: This is an Op-amp (IC TL084) based non-inverting variable gain amplifiers provided on board to amplify the recovered message singles i.e. output of the Low pass filter to desired level. Amplitude control is provided in circuit to vary the gain of the amplifier between 0 and 6.

4 Bit UP/DOWN Counter: This circuit is made using Synchronous 4-Bit Up/Down Counter with Mode Control IC 74LS191. The DM74LS191 circuit is a synchronous, reversible, up/down counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters. The outputs of the four master-slave flip-flops are triggered on a LOW-to-HIGH level transition of the clock input, if the enable input is LOW. A HIGH at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is HIGH. The direction of the count is determined by the level of the down/up input. When LOW, the counter counts up and when HIGH, it counts down.

4 Bit D/A converter: This has been constructed with a popular 8 bit D/A Converter IC DAC 0808. The DAC0808 is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 $I_{REF}/256$. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for I_{REF}[Greater Than Or Equal]2 mA. The power supply current of the DAC0808 is independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range. 4 LSB Bits are permanently grounded to make 4 bit converter. For complete specifications and operating conditions please refer the data sheet of DAC 0808.

DM Operation: The modulating signal is applied to buffer/signal shaping network. This applied signal will be super imposed by +1.5V DC so that the negative portion the modulating signal will clamped to positive, this process is needed, because input of the comparator should be between 0 and +3V.

After level shifting is done the signal will be passed to inverting input of the comparator. Non inverting input of the comparator is connected to output of the 4 Bit D/A converter. Comparator is operating at +5V single supply. So output of the comparator will be high (i.e +ve Vsat) when modulating signal is less than the reference signal i.e. D/A output, otherwise it will be 0 V. And this signal is transmitted as Delta Modulation signal. Same signal is also connected as UP/DOWN control to the UP/DOWN counter (74ls191).

UP/DOWN counter is programmed for 0000 starting count. So initially (i.e. when we switch on power supply) output of the counter is at 0000 and the D/A converter will be at 0V. Comparator compares the modulating signal and reference signal (D/A Output). Comparator output will be 0 if the modulating signal is greater than the reference signal. For next clock pulse depending on the UP/DOWN input (i.e. DM signal) counter will count up or down. If the UP/DOWN input is low (nothing but comparator output), counter will make up and output will be 0001. So the D/A converter will convert this 0001 digital input to equivalent analog signal (i.e. 0.3V 1 LSB Value). Now the reference signal is 0.3V, If still modulating signal is greater than the D/A output again comparator output (DM) will be low and UP count will occur. If not, DOWN count will take place. This process will continue till the reference signal and modulating signal voltages are equal. So DM signal is a series of 1 and 0.

DM signal is applied to a UP/DOWN input of the UP/DOWN counter at the receiver. This UP/DOWN counter is programmed for 1001 initial value (i.e. power on reset) and mode control is activated. So depend on the UP/DOWN input (DM Signal) for the next clock pulse counter will count UP or DOWN. This output is applied to 4 Bit D/A converter. A logic circuit is added to the counter which keeps the output of the counter in between 0000 and 1111 always. Output of the D/A converter will be a staircase signal lies between 0 and +4.7V. This stair case signal is applied a low pass filter. This low pass will smoothen the staircase signal so that original AF signal will be recovered.

We can use a voltage amplifier at the output of the low pass filter to amplify the recovered AF signal to desired voltage level.

Experimental procedure:

DM Modulator:

1. Connect the trainer (AET-73M) to the mains and switch on the power supply.
2. Observe the output of the AF generator using CRO, it should be a Sine wave of 100 Hz frequency with 3Vpp amplitude.
3. Observe the output of the Clock generator using CRO, they should be 4 KHz frequency of square wave with 5 Vp amplitude.

   Note**:** This clock signal is ***internally connected to the up/down counter*** so no external connection is required.
4. Connect AF signal from AF generator to the inverting input of the comparator and set output amplitude at 3Vpp.
5. Observe and plot the signals at D/A converter output (i.e., non-inverting input of the comparator), DM signal using CRO and compare them with the wave forms given in figure:3.
6. Connect DM signal to the DM input of the demodulator.
7. Connect clock (4 KHz) from modulator to the clock input of the demodulator. Connect clock input of the UP/DOWN counter to the clock from transmitter with the help of springs provided.
8. Observe and plot the output of the D/A converter and compare it with the wave forms given in Figure 1:3.
9. Connect D/A output to the LPF input.
10. Observe the output of the LPF/Amplifier and compare it with the original modulating signal.

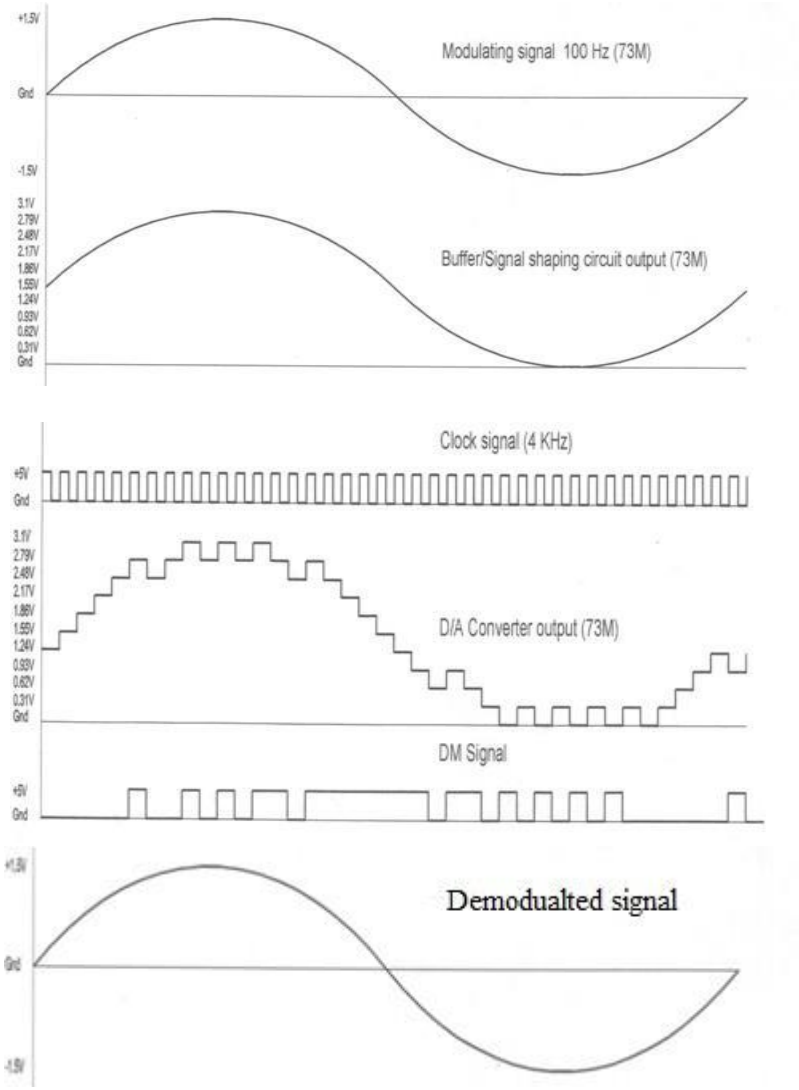


FIG: **Waveforms of DM with AC Voltage as modulating signal**

Observation table:-

Signal	Amplitude	Time Period	Frequency
AF Signal			
Transmitter Clk			
Demodulated signal			

Delta Modulation output: (Binary values)

RESULT:-

Questions:

1. How analog signal can be encoded in to bits?
2. What is the advantage of DM over PCM?
3. Which types of noise occur in delta modulation?
4. Define adaptive delta modulation.

Exp.No. 4	**FREQUENCY SHIFT KEYING** **MODULATION & DEMODULATION**
Dt.	

Aim: -To Study and observe the FSK modulation & demodulation techniques.

APPARATUS REQUIRED:
8 bit Variable Binary Data Generator (ST2111), Data Formatting and Carrier Modulation Transmitter Trainer (ST2106), Carrier Demodulation & Data Reformatting Receiver Trainer (ST2107), CRO, patch cards

Theory:
Frequency Shift Keying: In frequency shift keying, the carrier frequency is shifted in steps (i.e. from one frequency to another) corresponding to the digital modulation signal. If the higher frequency is used to represent a data '1' & lower frequency a data '0', the resulting Frequency shift keying waveform appears.

Block Diagram:

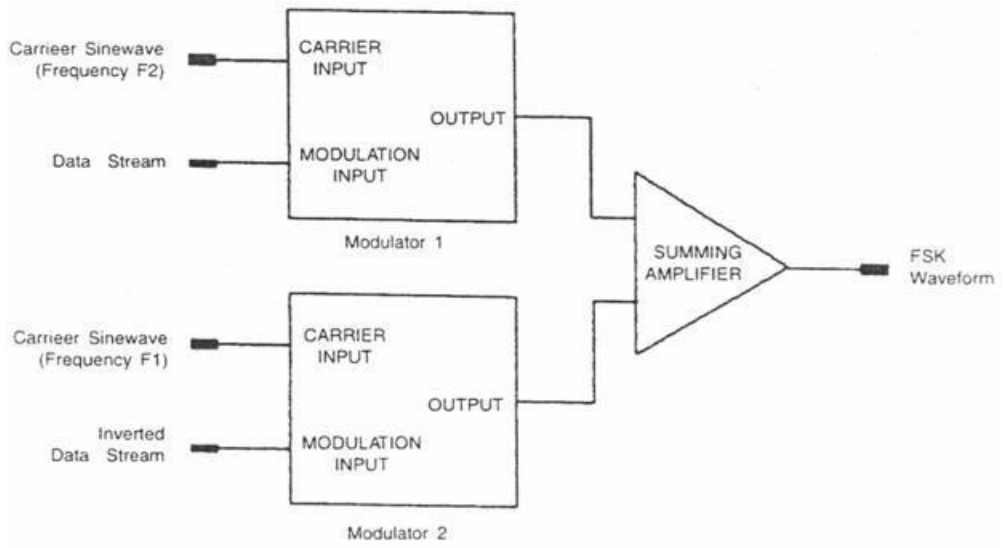


Fig1. Block diagram of FSK Modulator

FSK Modulator:

Since the amplitude change in FSK waveform does not matter, this modulation technique is very reliable even in noisy & fading channels. But there is always a price to be paid to gain that advantage. The price in this case is widening of the required bandwidth. The bandwidth increase depends upon the two carrier frequencies used & the digital data rate. Also, for a given data, the higher the frequencies & the more they differ from each other, the wider the required bandwidth. The bandwidth required is at least doubled than that in the ASK modulation. This means that lesser number of communication channels for given band of frequencies. Figure 1:1 shows the FSK modulator using IC XR 2206. IC XR 2206 is a VCO based monolithic function generator capable of producing Sine, Square, Triangle signals with AM and FM facility. In this trainer XR2206 is used generate FSK signal. Mark (Logic 1) and space (logic 0) frequencies can be independently adjusted by the choice of timing potentiometers F0 & F1. The output is phase continuous during transitions. The keying signal i.e. data signal is applied to pin 9.

FSK De-Modulator:

The demodulation of FSK waveform can be carried out by a phase locked loop. As known, the phase locked loop tries to 'lock' to the input frequency. It achieves this by generating corresponding output voltage to be fed to the voltage controlled oscillator, if any frequency deviation at its input is encountered. Thus the PLL detector follows the frequency changes & generates proportional output voltage. The output voltage from PLL contains the carrier components. Therefore the signal is passed through the low pass filter to remove them. The resulting wave is too rounded to be used for digital data processing. Also, the amplitude level may be very low due to channel attenuation. The signal is Squared Up' by feeding it to the voltage comparator. Figure shows the functional blocks involved in FSK demodulation. Figure 1:2 shows FSK Demodulator, is a combination of PLL (LM565) and comparator (Op-amp). The frequency-changing signal at the input to the PLL drives the phase detector to result in rapid change in the error voltage, which is applied to the input of the comparator. At the space frequency, the error voltage out of the phase detector Is below the comparison voltage of the comparator. The comparator is a non-inverting circuit, so its output level is also low. As the phase detector input frequency shifts low (to the mark frequency), the error voltage steps to a high level, passing through the comparison level, causing the comparator output voltage to go high. This error voltage change will snap the comparator output voltage between its two output levels in manner that duplicates the data signal input to the XR2206 modulator.

The free running frequency of the PLL (no input signal) is set midway between the mark and space frequencies. A space at 2025 Hz and mark at 2225 Hz will have a free running VCO frequency of 2125 Hz.

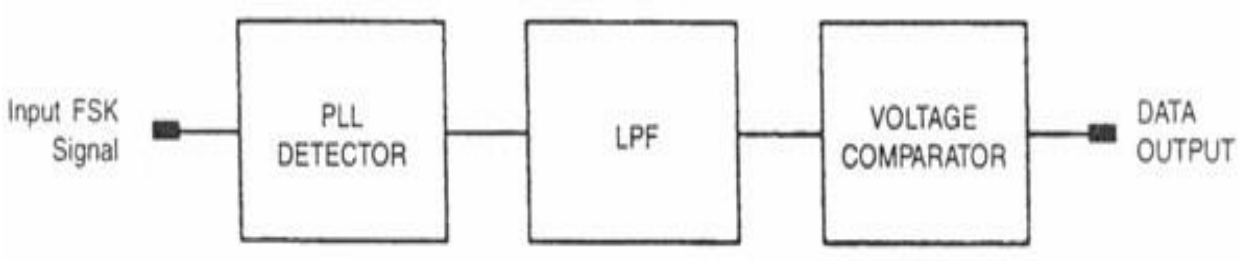


Fig.2: Block diagram of FSK DEMODULATOR

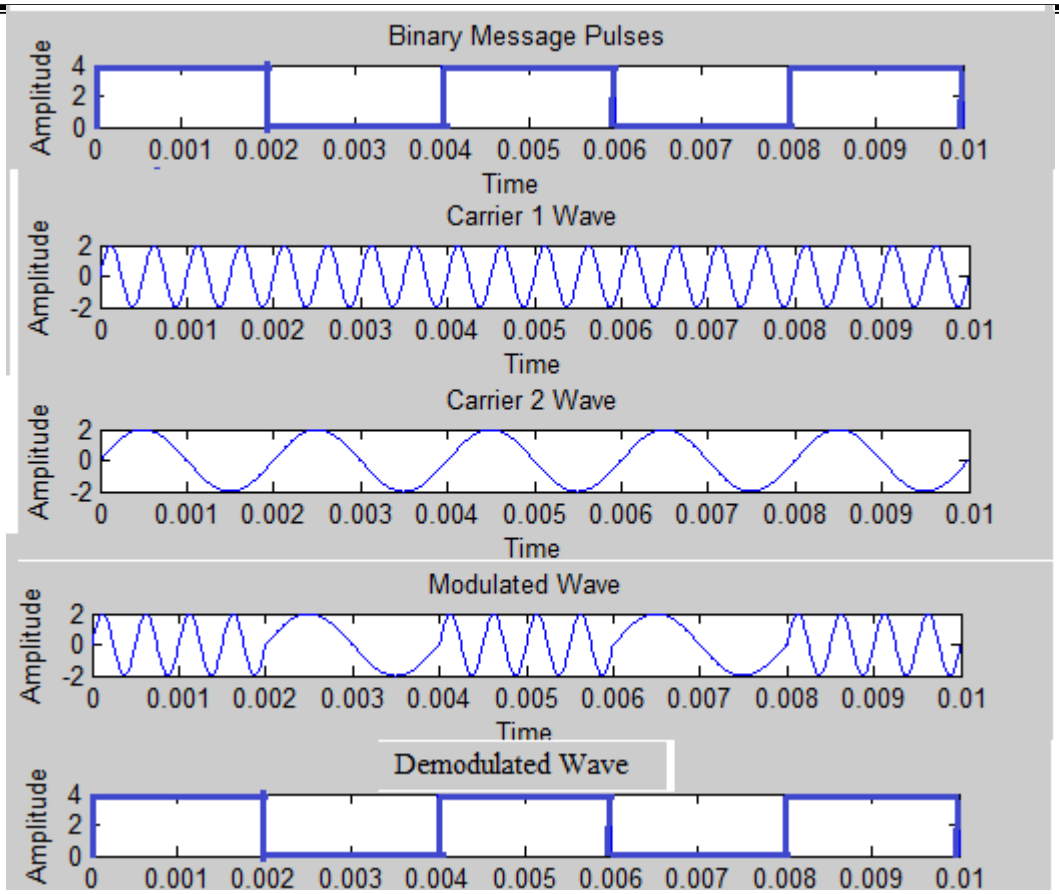


Fig 3: Waveforms of FSK

Experimental procedure:

FSK Modulation:

1. Connect output of the logic source to data input of the FSK Modulator.
2. Set logic source switch in 0 position.
3. Connect FSK modulator output to Oscilloscope as well as frequency counter.
4. Set the output frequency of the FSK modulator as per your desire (say 0-1.2 KHz) with the help of control F0 which represents logic 0.
5. Set logic source switch in 1 position.
6. Set the output frequency of the FSK modulator as per your desire (say 2-3 KHz) with the help of control F1 which represents logic 1.

   Note: We have chosen F0 as 1.2 KHz and F1 as 2.4 KHz for ease of operation, in fact you may set any value.

7. Now connect data input of the FSK modulator to the output of the data signal generator.
8. Keep CRO in dual mode connect CH1 input of the oscilloscope to the input of the FSK modulator and CH2 input to the output of the FSK modulator.
9. Observe the FSK signal for different data signal frequencies and plot them. By this we can observe that the carrier frequency is shifting between two predetermined frequencies as per the data signal i.e. 0-1.2 KHz when data signal is 0 and 2-3 KHz when data input is 1 in this case.

10. Compare these plotted wave forms with the theoretically drawn in figure 3.

FSK Demodulation:

11. Now connect the FSK modulator output to the FSK input of the demodulator.
12. Connect CH1 input of the Oscilloscope to the data signal at modulator and CH2 input to the output of the FSK demodulator (keep CRO in dual mode).
13. Observe and plot the output of the FSK demodulator for different frequencies of data signal. Compare the original data signal and demodulated signal; by this we can observe that there is no loss in process of FSK modulation and demodulation.

OBSERVATION TABLE:

Signal	Amplitude	Frequency
Data signal		
Carrier 1		
Carrier 2		
Data at receiver o/p		

Frequency of FSK output of Logic 1:
Frequency of FSK output of Logic 0:

SOFTWARE PROCEDURE:

1. Switch ON the power supply
2. Open MATLAB software by clicking MATLAB icon on Desktop.
3. Open the editor window and write the program on it.
4. Save the program in workspace as .m file.
5. Run the program and view the graph.

MATLAB CODE:

```
clc%for clearing the command window
close all%for closing all the window except command window
clear all%for deleting all the variables from the memory
fc1=input('Enter the freq of 1st Sine Wave carrier:');
fc2=input('Enter the freq of 2nd Sine Wave carrier:');
fp=input('Enter the freq of Periodic Binary pulse (Message):');
amp=input('Enter the amplitude (For Both Carrier & Binary Pulse Message):');
amp=amp/2;
% For setting the sampling interval
t=0:0.00001:0.01;
c1=amp.*sin(2*pi*fc1*t);% For Generating 1st Carrier Sine wave
c2=amp.*sin(2*pi*fc2*t);% For Generating 2nd Carrier Sine wave
subplot(4,1,1); %For Plotting The Carrier wave
plot(t,c1)
xlabel('Time')
ylabel('Amplitude')
```

```
title('Carrier 1 Wave')
subplot(4,1,2) %For Plotting The Carrier wave
plot(t,c2)
xlabel('Time')
ylabel('Amplitude')
title('Carrier 2 Wave')
m=amp.*square(2*pi*fp*t)+amp;%For Generating Square wave message
subplot(4,1,3) %For Plotting The Square Binary Pulse (Message)
plot(t,m)
xlabel('Time')
ylabel('Amplitude')
title('Binary Message Pulses')
for i=0:1000; %here we are generating the modulated wave
if  m(i+1)==0
        mm(i+1)=c2(i+1);
else
        mm(i+1)=c1(i+1);
end
end
subplot(4,1,4) %For Plotting The Modulated wave
plot(t,mm)
xlabel('Time')
ylabel('Amplitude')
title('Modulated Wave')
```

RESULT:-

VIVA- QUESTIONS:

1. Why FSK is preferred over ASK?
2. What is BFSK?
3. What is the difference between FM and FSK?
4. What is the bandwidth of BFSK?
5. What is the disadvantage of BFSK?

Exp.No. 5	DIFFERENTIAL PHASE SHIFT KEYING
Dt.	

AIM: To Study the DPSK modulator and Demodulator.

EQUIPMENT REQUIRED:

1. Differential phase shift keying trainer
2. Storage oscilloscope
3. Digital multiplexer
4. 2 No's of co-axial cables

BLOCK DIAGRAMS:

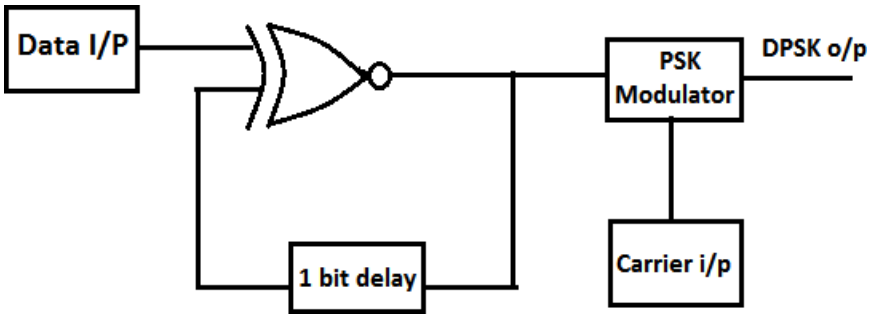


Fig 1:DPSK Modulator

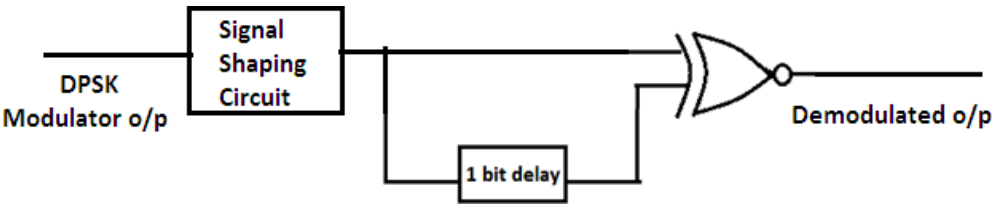


Fig 2: DPSK Demodulator

INTRODUCTION

THEORY:

PSK: Phase shift keying is a modulation/ Data transmitting technique in which the phase of the carrier signal is shifted between two distinct levels. In a simple PSK (i.e. Binary PSK) and shifted carrier VCos W_0t is transmitted to indicate a 1 condition, and the carrier shifted by 180^o i.e. –VCos w_0t is transmitted to indicate as 0 condition.

DPSK: phase shift keying requires a local oscillator at the receiver which is accurately synchronized in phase with the unmodulated transmitted carrier, and in practice this can be difficult to achieve. **Differential phase shift keying (DPSK)** overcomes the difficulty by combining two basic operations at the transmitter. (1) Differential encoding of the input binary wave and (2) phase shift keying- hence, the name differential phase shift keying. In other words, DPSK is a man coherent version of the PSK.

The differential encoding operation performed by the modulator has explained below. Let b' (t) be the binary message to be transmitted. An encoded message stream b(t) is generated from b'(t) by using a

logic circuit. The first bit in b(t) is arbitrary which may be chosen as 1 or 0. The subsequent bit in b(t) are determined on the basis of the rule that when b'(t) is 1. b(t) does not change its value and, when b'(t) is 0, b(t) changes its value. The below table shows the two possible bit streams b(t) and the respective phases. In the first bit stream, the initial bit(arbitrary) is 1 and, in the second bit stream, the initial bit is 0.EX-NOR gate can be used to perform this operation as its output is a 1 when both the inputs are same, and a 0 when the inputs are different.

TABLE 1

Example for complete DPSK operation (with arbitrary bit as 0)

Message signal(to be transmitted)	0	1	1	0	0	
Encoded data(differential data)	0	1	1	1	0	1
Transmitted signal phase	180	0	0	0	180	0
Received signal phase	180	0	0	0	180	0
Message signal(demodulated)		0	1	1	0	0

DPSK Modulator:

The above figure 1 shows the DPSK modulator. This consists of PSK modulator and differential encoder.

PSK modulator: IC CD 4052 is a 4 channel analog multiplexer and is used as an active component in the circuit. One of the control signals of 4052 is grounded so that 4052 will act as a 2 channel multiplexer and other control is being connected to the binary signal i.e. encoded data. Unshifted carrier signal is connected directly to channel 1 and carrier shifted by 180^0 is connected to channel 2. Phase shift network is a unity gain-inverting amplifier using OP AMP (TL084).

` When control signal is at high voltage, output of the 4052 is connected to channel 1 and unshifted (or 0 phase) carrier is phased on to output. Similarly, when control signal is at zero voltage output of 4052 is connected to channel 2 and carrier shifted by 180^o is phased on to output.

Differential encoder: this consists of 1 bit delay circuit and an EX-NOR gate. 1 bit delay circuit is formed by a D- latch. Data signal i.e. signal to be transmitted is connected to one of the input of the EX-NOR gate and other one being connected to out of the delay circuit. Output of the EX-NOR gate is connected to control input of the multiplexer (IC 4052) and as well as to input of the D-Latch. Output of the EX-NOR gate is 1 when both the inputs are same and it is 0 when both the inputs are different.

DPSK Demodulator:

The above figure 2 shows the DPSK demodulator. This consists of 1 bit delay circuit, EX-NOR gate and a signal shaping circuit. Signal shaping circuit consists of an OP-Amp based zero crossing detector followed by a D-Latch. Received DPSK signal is converted to square wave with help of zero crossing and this square wave will pass through the D-latch. Therefore, output of the D-Latch is an encoded data. This encoded data is applied to 1 bit delay circuit as well as to one of the inputs of EX-NOR gate. And output of the delay circuit is connected to another input of the EX-NOR gate. Output of the EX-NOR gate is one when both the inputs are same and it is 0 when both the inputs are different.

Experimental procedure:

Modulator:

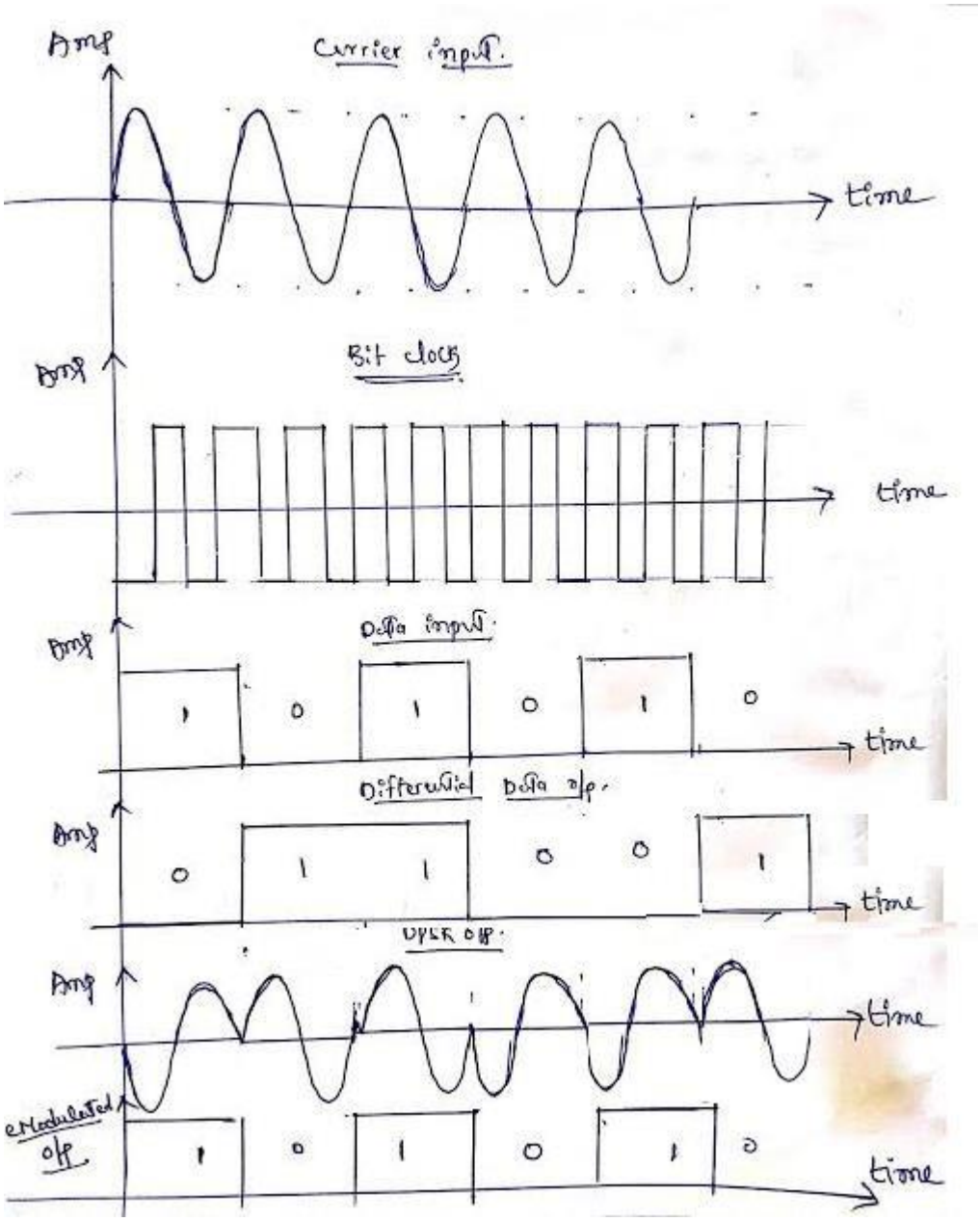
1. Connect the trainer to mains and switch on the power supply
2. Observe the output of the carrier generator using CRO, it should be an 8 KHZ sine with 5V PP amplitude.
3. Observe the data signal from data source using CRO and this will be a TTL compatible signal of following sequence.

   10101101001010110100
4. Observe the output of clock generator using CRO. It should be a square wave of 4 KHZ frequency with 5V peak amplitude.
5. Connect carrier signal to carrier input of the PSK modulator.
6. Connect data signal from data source to data input of the EX-NOR gate.
7. Keep CRO in dual mode.
8. Connect channel 1 input of the CRO to data signal and channel 2 input to the encoded data. (which is nothing but the output of the EX-NOR gate)
9. Observe the encoded data with respect to data input. The encoded data will be the given sequence.
   Actual data signal: 10101101001010110100
   Encoded data signal: 01100011011001110010
10. Now connect channel 2 input of the CRO to the DPSK output and channel 1 input to the encoded data. Observe the input and output wave forms and plot the same
11. Compare the plotted waveforms with the given waveforms.

Demodulation:

12. Connect DPSK signal to the input of the signal shaping circuit from DPSK transmitter with the help of co-axial cable.
13. Connect clock from the transmitter to clock input of the one bit delay circuit using co-axial cable.
14. Keep CRO in dual mode. Connect channel 1 input to the encoded data (at modulator) and channel 2 input to the encoded data (at demodulator).
15. Observe an plot both the waveforms and compare it with the given waveforms. You will notice that both the signals are same with 1 bit delay
16. Keep CRO in dual mode. Connect channel 1 input to the data signal (at modulator) and channel 2 input to the output of the demodulator.
17. Observe an plot both the waveforms and compare it with the given waveforms. You will notice that both the signals are same with 1 bit delay
18. Disconnect the clock from transmitter and connect to local oscillator clock with remaining setup as it is. Observe demodulator output and compare it with the previous output.

EXPECTED WAVEFORMS:



RESULTS:

VIVA QUESTIONS:-

1 what is PSK?
2 What is the disadvantage of PSK?
3 What is BPSK?
4 How BPSK is generated?
5 what is the advantage of PSK?

Exp.No. 6	**Sampling Theorem**
Dt.	

AIM :-To study the Sampling theorem using MATLAB.

APP ARATUS REQUIRED :- MATLAB R2016a

PROCEDURE:

1. Switch ON the power supply
2. Open MATLAB software by clicking MATLAB icon on Desktop.
3. Open the editor window and write the program on it.
4. Save the program in workspace as .m file.
5. Run the program and view the graph.

MATLAB CODE:

```
Close all;
Clear all;
t=-10:0.01:10;
T=8;
fm=1/T;
x=cos(2*pi*fm*t);
fs1=1.2*fm;
fs2=2*fm;
fs3=8*fm;
n1=-5:1:5;
xn1=cos(2*pi*n1*fm/fs1);
subplot(221)
plot(t,x);
xlabel('time in seconds');
ylabel('x(t)');
title('continous time signal');
subplot(222)
stem(n1,xn1);
hold on;
plot(n1,xn1);
xlabel('n');
ylabel('x(n)');
title('discrete time signal with fs<2fm');
n2=-5:1:5;
xn2=cos(2*pi*n2*fm/fs2);
subplot(223)
stem(n2,xn2);
hold on;
plot(n2,xn2);
xlabel('n');
```

```
ylabel('x(n)');
title('discrete time signal with fs=2fm');
n3=-5:1:5;
xn3=cos(2*pi*n3*fm/fs3);
subplot(224)
stem(n3,xn3);
hold on;
plot(n3,xn3);
xlabel('n');
ylabel('x(n)');
title('discrete time signal with fs>2fm');
```

Result:

VIVA QUESTIONS:

1) Define Sampling Theorem
2) Define Nyquist Rate
3) Define Energy of a Signal
4) Define Power of a signal.

Exp.No. 7	PHASE SHIFT KEYING
Dt.	

AIM: To study the operation of Phase shift keying using MATLAB.

Apparatus Required: MATLAB R2016a

PROCEDURE:

1. Switch ON the power supply
2. Open MATLAB software by clicking MATLAB icon on Desktop.
3. Open the editor window and write the program on it.
4. Save the program in workspace as .m file.
5. Run the program and view the graph.

MATLAB CODE:

```
Clear all;
clc;
close all;
set(0,'defaultlinelinewidth',2);
A=5;
t=0:0.00001:0.01;
f1=input('Carrier Sine wave frequency =');
f2=input('Message frequency =');
x=A.*sin(2*pi*f1*t);%Carrier Sine
subplot(3,1,1);
plot(t,x);
xlabel('time');
ylabel('Amplitude');
title('Carrier');
grid on;
u=square(2*pi*f2*t);%Message signal
subplot(3,1,2);
plot(t,u);
xlabel('time');
ylabel('Amplitude');
title('Message Signal');
grid on;
v=x.*u;%Sine wave multiplied with square wave
subplot(3,1,3);
plot(t,v);
axis([0 0.01 -6 6]);
xlabel('t');
ylabel('y');
title('PSK');
grid on;
```

Result:

VIVA QUESTIONS:

1. Compare FSK and PSK.
2. List the Characteristics of TL084 op-amp.
3. Compare TL084 op amp with IC 741 op amp.
4. What do we infer from constellation diagrams of various modulation schemes?

Exp.No. 8	**DIFFERENTIAL PULSE CODE MODULATION**
Dt.	

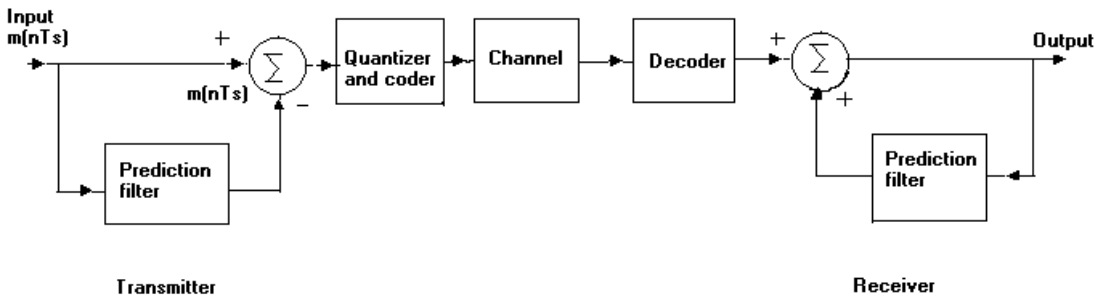
AIM : To analyze a DPCM system and to interpret the modulated and demodulated waveforms

APPRATUS:

1. DPCM Modulation and Demodulation Trainer Kit
2. Dual Trace oscilloscope
3. Digital Multimeter
4. C.R.O (30MHz)
5. Patch chords.

BLOCK DIAGRAM:

Block diagram of DPCM



THEORY:

Differential PCM is quite similar to ordinary PCM. However, each word in this system indicates the difference in amplitude, positive or negative, between this sample and the previous sample. Thus the relative value of each sample is indicated rather than, the absolute value as in normal PCM. This unique system consists of

I. DPCM Modulator

1. Regulated power supply
2. Audio Frequency signal generator
3. Prediction Filter Sample & Hold circuit
4. A/D Converter
5. Parallel –Serial Shift register
6. Clock generator / Timing circuit
7. .DC Source

II. DPCM Demodulator

1. Regulated Power Supply

2. Serial-Parallel Shift registers.

3. D/A converter.

4. Clock generator

5. Timing circuit

6. Prediction filter

7. Passive low pass filter

PROCEDURE:

1. Study the theory of operation thoroughly.

2. Connect the trainer (Modulator) to the mains and switch on the power supply.

3. Observe the output of the AF generator using CRO, it should be Sine wave of 400 Hz frequency with 3V pp amplitude.

4. Verify the output of the DC source with multi-meter/scope; output should vary 0 to +290mV.

5. Observe the output of the Clock generator using CRO, they should be 64 KHz and 8 KHz frequency of square with 5 Vpp amplitude.

6. Connect the trainer (De Modulator) to the mains and switch on the power supply.

7. Observe the output of the Clock generator using CRO; it should be 64 KHz square wave with amplitude of 5 pp.

DPCM Operation (with DC input):

Modulation:

8. Keep CRO in dual mode. Connect one channel to 8 KHz signal (one which is connected to the Shift register) and another channel to the DPCM output.

9. Observe the DPCM output with respect to the 8 KHz signal and sketch the waveform.

10. Note: Form this waveform you can observe that the LSB bit enters the output first.

11. Set DC source to some value say 1 V with the help of multi-meter and connect it to the A/D converter input and observe the output LED's.

Demodulation

1. Connect DPCM signal to the demodulator (S-P register) from the DPCM modulator with the help of coaxial cable (supplied with the trainer).

2. Connect clock signal (64 KHz) from the transmitter to the receiver using coaxial cable.

3. Connect transmitter clock to the timing circuit.

4. Observe and note down the S-P shift register output data and compare it with the transmitted data (i.e. output A/D converter at transmitter) notice that the output of the S-P shift register is

following the A/D converter output in the modulator.

5. Observe D/A converter output (demodulated output) using multi-meter/scope and compare it with the original signal and can observe that there is no loss in information in process of conversion and transmission.

DPCM Operation (with AC input):

Modulation:

6. Connect AC signal of 3VPP amplitude to positive terminal of the summer circuit.

Note: The output of the prediction filter is connected to the negative terminal of the summer circuit and can observe the waveforms at the test points provided on the board.

7. The output of the summer is internally connected to the sample and hold circuit

8. Keep CRO in dual mode. Connect one channel to the AF signal and another channel to the Sample and Hold output. Observe and sketch the sample & hold output

9. Connect the Sample and Hold output to the A/D converter and observe the DPCM output using oscilloscope.

10. Observe DPCM output by varying AF signal voltage.

Demodulation:

11. Connect DPCM signal to the demodulator input (S-P shift register) from the DPCM modulator with the help of coaxial cable (supplied with trainer).

12. Connect clock signal (64 KHz) from the transmitter to the receiver using coaxial cable.

13. Connect transmitter clock to the timing circuit.

14. Keep CRO in dual mode. Connect one channel to the sample & hold output and another channel to the D/A converter output.

15. Observe and sketch the D/A output

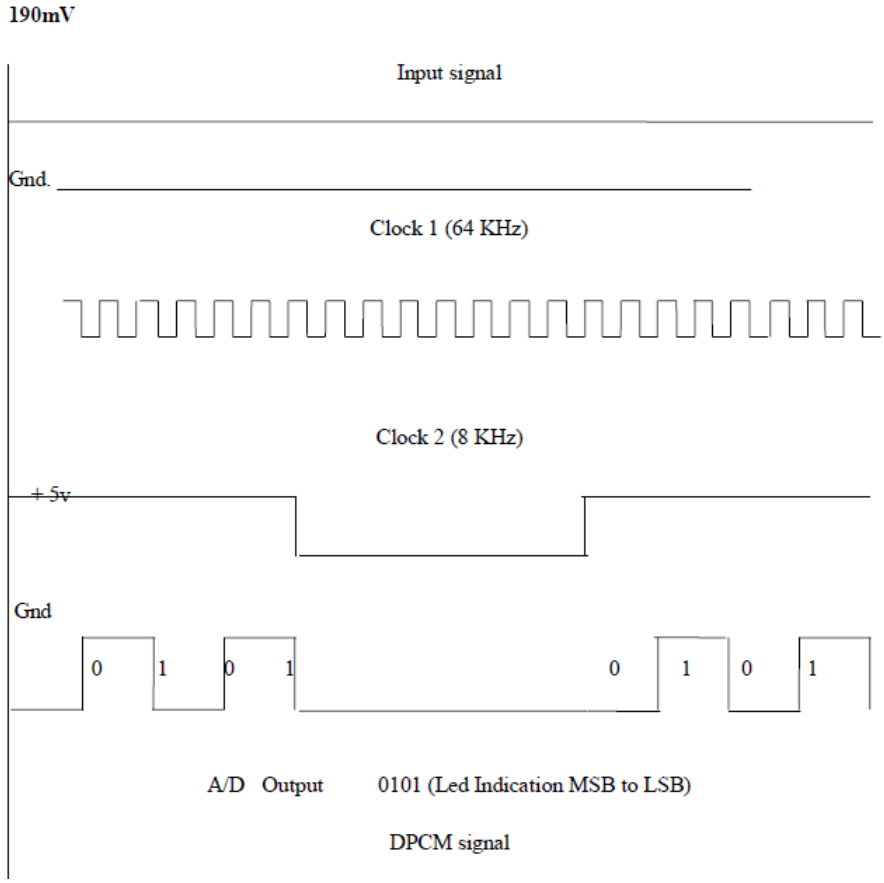
16. Connect D/A output to the LPF input and observe the output of the LPF.

17. Observe the wave form at the output of the summer circuit.

18. Disconnect clock from transmitter and connect to the local oscillator (i.e., clock generator output from De Modulator) with remaining setup as it is. Observe D/A output and compare it with the previous result. This signal is little bit distorted in shape. This is because lack of synchronization between clock at transmitter and clock at receiver.

EXPECTED WAVEFORMS:

Draw the wave forms for the given DC input, corresponding binary data wave form, and for AC input draw sample and hold waveform then D/A converter o/p and then reconstructed AC signal



OBSERVATIONS: DPCM with AC input

	Amplitude	Time period
AC Input		
Prediction Filter Output		
Sample and Hold Output		
Clock -1 output		
DPCM Output		

Demodulation:

	Amplitude	Time period
DPCM Input		
D/A Converter Output		
LPF Output		
Demodulation Output		
Prediction Filter output		

CODE FOR DEFFERENTIAL PULSE CODE MODULATION

```
clear all
close all
clc
fid=fopen('speech_dft.mp3','r');
[m,count]=fread(fid,'int16');
count=8500;
fs=8000;
ts=1;
no_samples=(2*fs)+ts;
time=[1:fs/64];
mp=max(m);
bits=5;
levels=2^bits;
bit_rate=8000*bits;
alpha=0.45;
diff_sig(1)=m(1);
for k=2:count,
   diff_sig(k)=m(k)-alpha*m(k-1);
end
dp=max(diff_sig)
stepsize=(2*mp)/levels
for k=1:no_samples,
   samp_in(k)=m(k*ts);
   quant_in(k)=samp_in(k)/stepsize;
   error(k)=(samp_in(k)-quant_in(k))/no_samples;
end
signs=sign(m);
quant_out=quant_in;
for i=1:count,
   s(i)=abs(quant_in(i))+0.5;
   quant_out(i)=signs(i)*round(s(i))*stepsize;
end
s_out=quant_out;
s_out(1)=quant_out(1);
for k=2:count,
   s_out(k)=quant_out(k)+alpha*s_out(k-1);
end
nq=(((stepsize)^2)/12)*((mp/dp)^2)
snr=1.5*(levels^2)
snr_db=10*log10(snr)
subplot(4,1,1);
plot(time,m(time),time,s_out(time),'r');
title('input speech signal');
xlabel('time');
ylabel('m(t)');
grid on;
subplot(4,1,2);
plot(time,quant_in(time),'r');
title('quantized speech signal');
xlabel('time');
ylabel('levels');
grid on;
```

```
subplot(4,1,3);
plot(time,s_out(time));
title('decoded dpcm speech signal');
xlabel('time');
ylabel('dq(t)');
grid on;
subplot(4,1,4);
plot(time,error(time));
title('error signal');
xlabel('time');
ylabel('error(t)');
grid on;
clear all
```

RESULT:

Thus the Differential Pulse code modulation and demodulation were performed.

VIVA QUESTIONS:

1. For data compression says whether ADPCM or DPCM is better. Justify.
2. What is the need for compression? Mention the types of compression.
3. List the communication standards which use DPCM.
4. Based upon the knowledge that you have gained after doing the experiment write the Functions of sample and hold circuit.
5. Name the circuit used to achieve synchronization between transmitter and receiver.

Exp.No. 9	**QPSK GENERATION AND DETECTION**
Dt.	

AIM: To study modulation and demodulation of QPSK and sketch the relevant waveforms.

APPRATUS:

1. QPSK Trainer Kit
2. Dual Trace oscilloscope
3. Digital Multimeter
4. C.R.O (30MHz)
5. Patch chords.

THEORY:

The Quadrature Phase Shift Keying QPSKQPSK is a variation of BPSK, and it is also a Double Side Band Suppressed Carrier DSBSCDSBSC modulation scheme, which sends two bits of digital information at a time, called as bigits. Instead of the conversion of digital bits into a series of digital stream, it converts them into bit pairs. This decreases the data bit rate to half, which allows space for the other users

BLOCK DIAGRAM: QPSK MODULATOR & DEMODULATOR

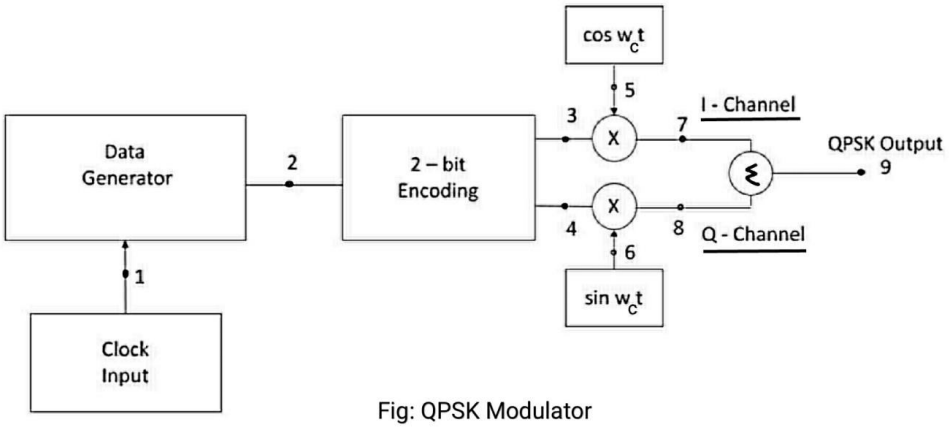


Fig: QPSK Modulator

PROCEDURE:

1. Connect and switch on the power supply.
2. QPSK is selected by default and LEDs of corresponding technique will glow.
3. Select the bit pattern using push button i.e. 8 bit or 16 bit or 32 bit or 64 bit. Observe bit pattern on TP-2.
4. Select data rate using push button i.e. 2 KHz or 4 KHz or 8 KHz 16 KHz.

Modulation:

5. Observe the input bit pattern at TP-2 by varying bit pattern using respective push button.
6. Observe the data rate at TP-1 by varying data rate using respective push button.
7. Observe the Two- bit encoding i.e. I-Channel (TP-3) and Q-Channel (TP-4).
8. Observe carrier signal i.e. cosine wave (TP-5) and sine wave (TP-6). Frequency of carrier signal will change with respect to data rate.

9. Observe I-Channel (TP-7) and Q-Channel (TP-8) modulated signal.

10. Observe QPSK modulated signal at TP-9.

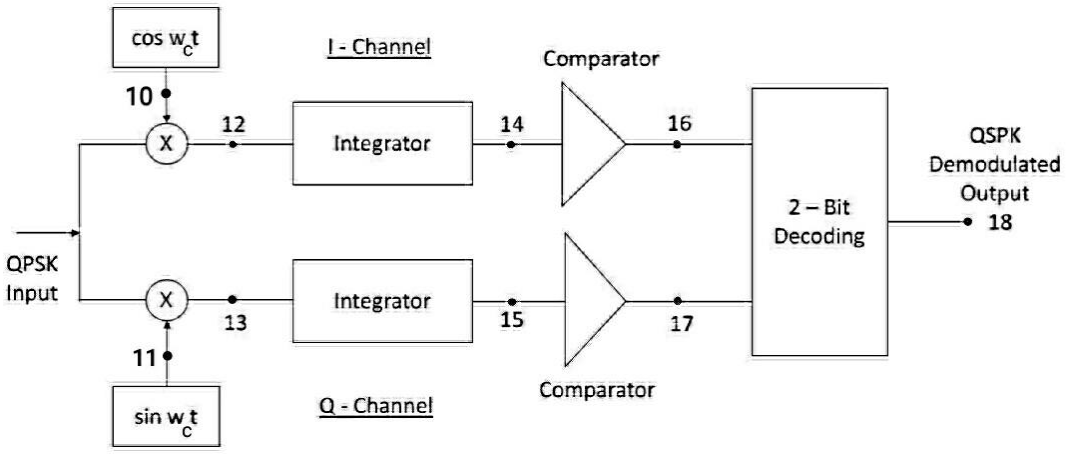


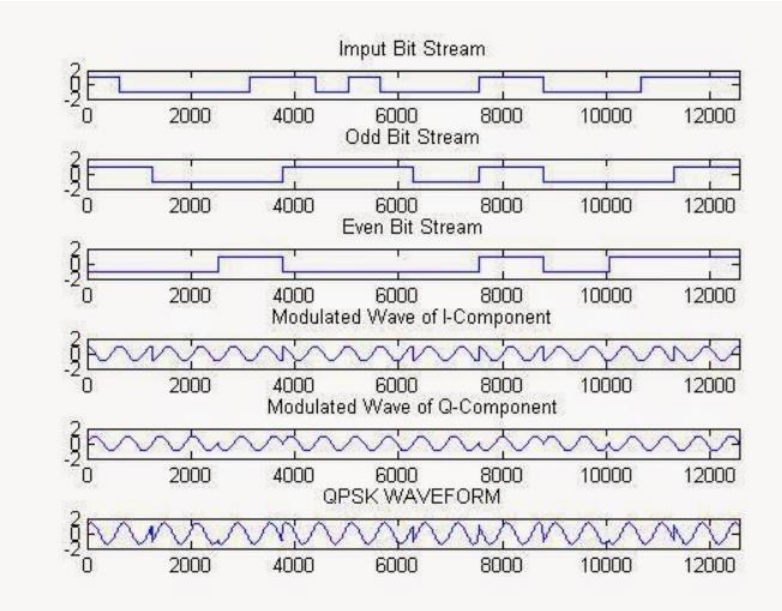
Fig: QPSK Demodulator

Demodulation:

11. Apply the QPSK modulated output to the demodulator input.
12. Observe the multiplied signal of QPSK and carrier signal, cosine at TP-12 and also observe the multiplied signal of QPSK and carrier signal, sine at TP-13.
13. Observe the integrated output at I-channel (TP-14) and Q-channel (TP-15).

Input Bits	Phase of QPSK signal	Co –ordinates of message signal	
		S1	S2
10	**π/4**		
00	**3π/4**		
01	**5π/4**		
11	**7π/4**		

EXPECTED WAVE FORMS:



CODE FOR QPSK GENERATION

```
clear all
close all
clc
data=input('Enter the data for qpsk');
last = length(data);
t=1;
for start = 1:last

   if (data(start)==0)     %% 00
      for j=0:0.1:19.9
         q(t)=0;
         o(t)=sin(j);    %% 0 degree
         t=t+1;
      end

   elseif (data(start)==1) %% 01
      for j=0:0.1:19.9
         q(t)=1;
         o(t)=cos(j);    %% 90 degree
         t=t+1;
      end

   elseif (data(start)==10) %% 10
      for j=0:0.1:19.9
         q(t)=2;
         o(t)=-sin(j);   %% 180 degree
         t=t+1;
      end

   else %(data(start)==11) %% 11
      for j=0:0.1:19.9
         q(t)=3;
         o(t)=-cos(j);   %% 270 degree
         t=t+1;
      end
   end
end
subplot(2,1,1)
plot(q);
title('INPUT');
subplot(2,1,2)
plot(o);
title('OUTPUT');
```

RESULT: QPSK modulation and demodulation wave forms are observed.

VIVA QUESTIONS:

1. Draw the constellation diagram of QPSK.
2. Give some applications of QPSK modulation scheme
3. Find the output of the following command. 5^ (2/3) – 25/ (2*3)
4. What is the relationship between 4 QAM and QPSK?
5. Design a SIMULINK model for QPSK.